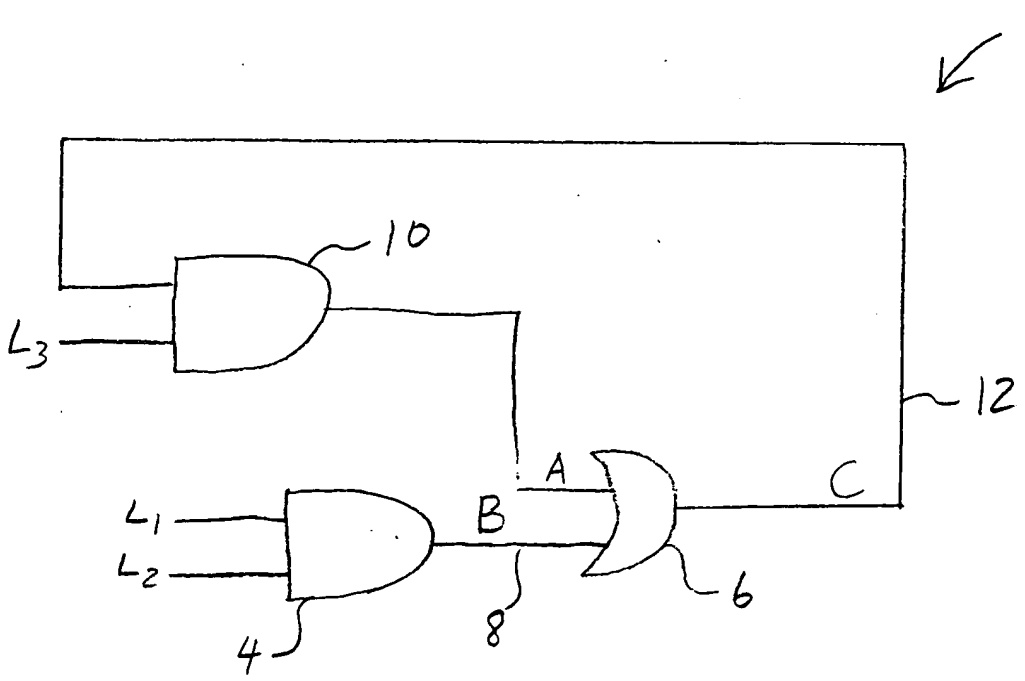


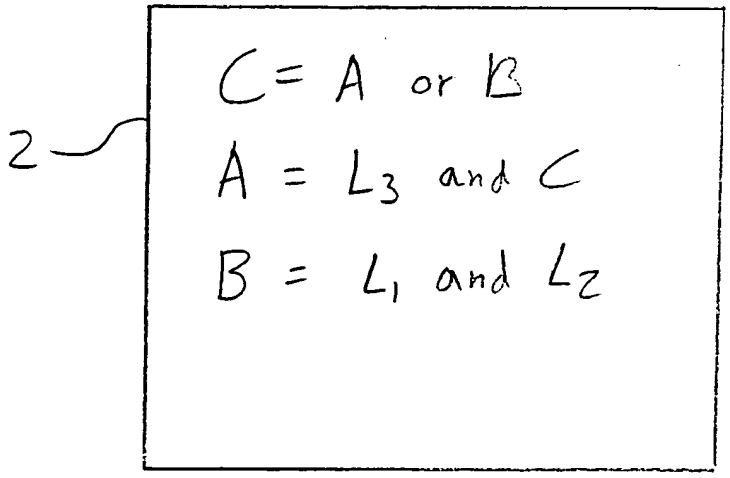


Fig. 1
(Prior Art)

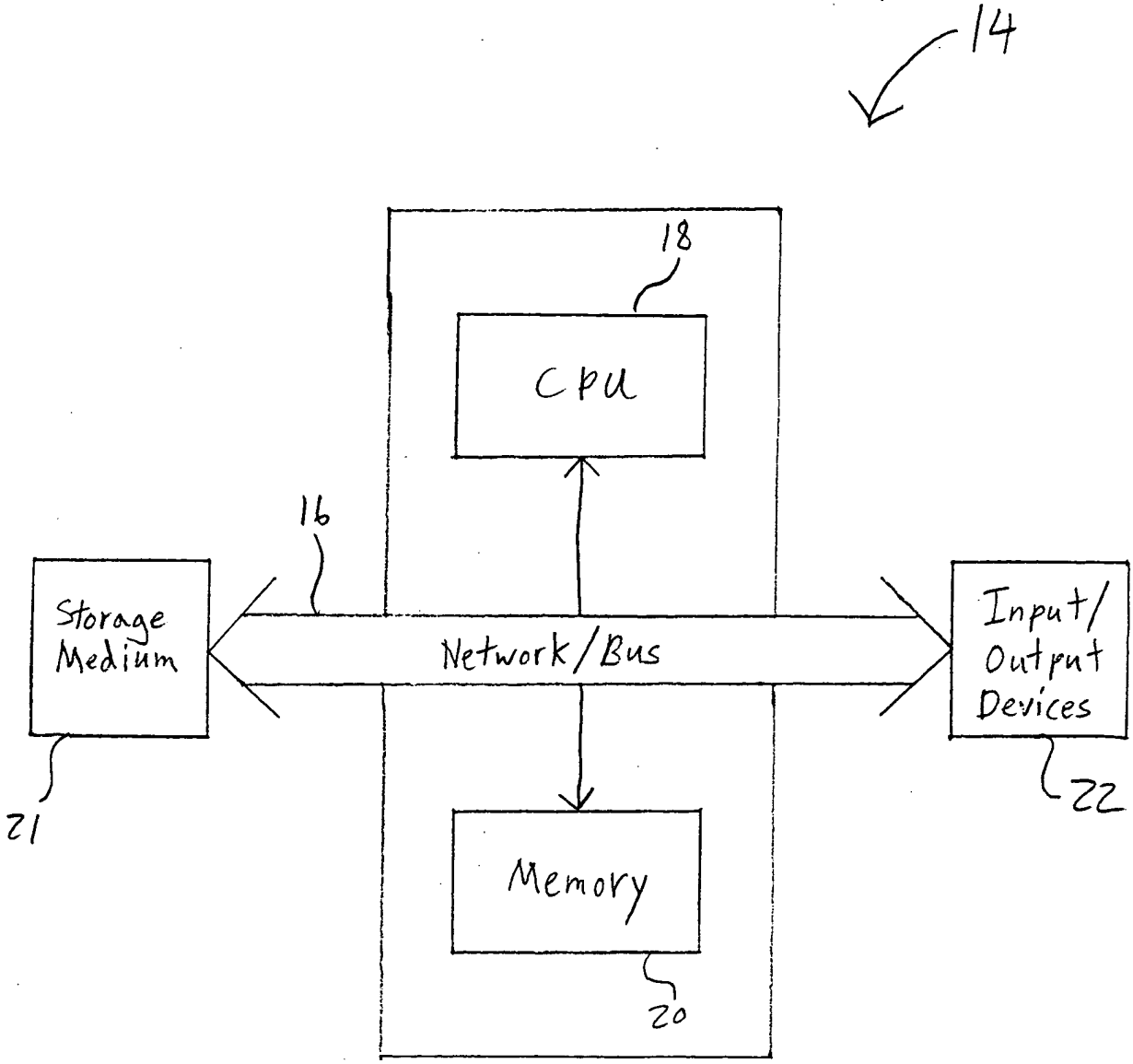
14
18
CPU
16
Storage Medium
Network/Bus
Input/ Output Devices
21
22
Memory
20

Fig. 2

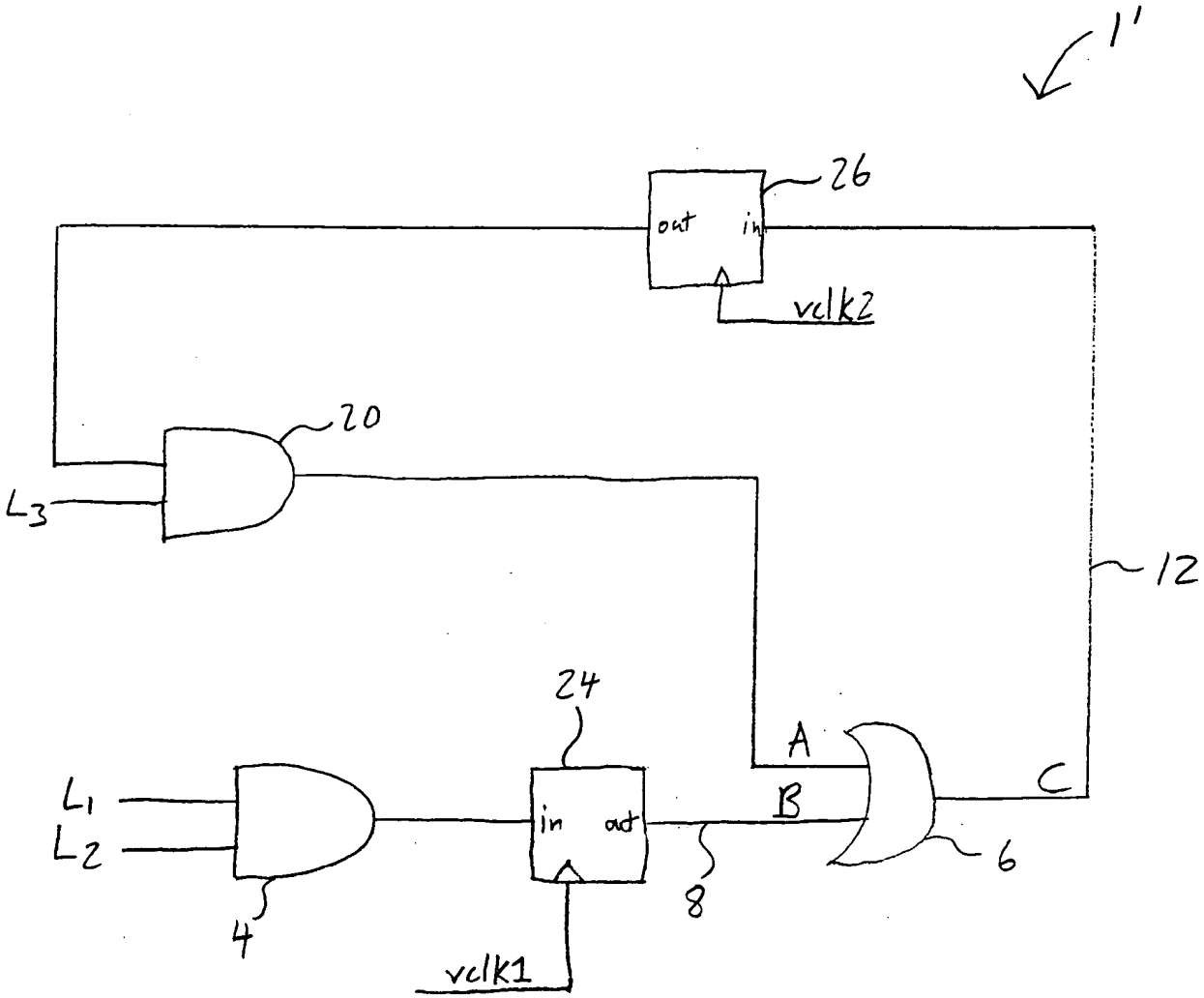


Fig. 3A

$in_{24}$ = $L_1$ and $L_2$
$out_{24}$ = if (vclk1 == HIGH) then $in_{24}$//change state
else $out_{24}$//retain state
B = $out_{24}$
C = A or B
$in_{26}$ = C
$out_{26}$ = if (vclk2 == high) then $in_{26}$//change state
else $out_{26}$//retain state
A = $L_3$ and $out_{26}$

~27

```
module fig1 ( L1, L2, L3, vclk1, vclk2, .. )
input L1, L2, L3, vclk1, vclk2;

        and     g14 ( in24, L1, L2 );
        vdelement g24 ( out24, vclk1, in24 );
        or      g16 ( in26, A, out24 );
        vdelement g26 ( out26, vclk2, in26 );
        and     g20 ( A, L3, out26 );

endmodule


primitive vdelement (out, vclk, in)
output out;
reg out;
input vclk, in;

table
// vclk  data   out     out_new
  1      1 :    ?       : 1 ;
  1      0 :    ?       : 0 ;
  0      ? :    ?       : - ; // - means 'no change', i.e. retain previous value
endtable
endprimitive
```

~28

Fig. 3B

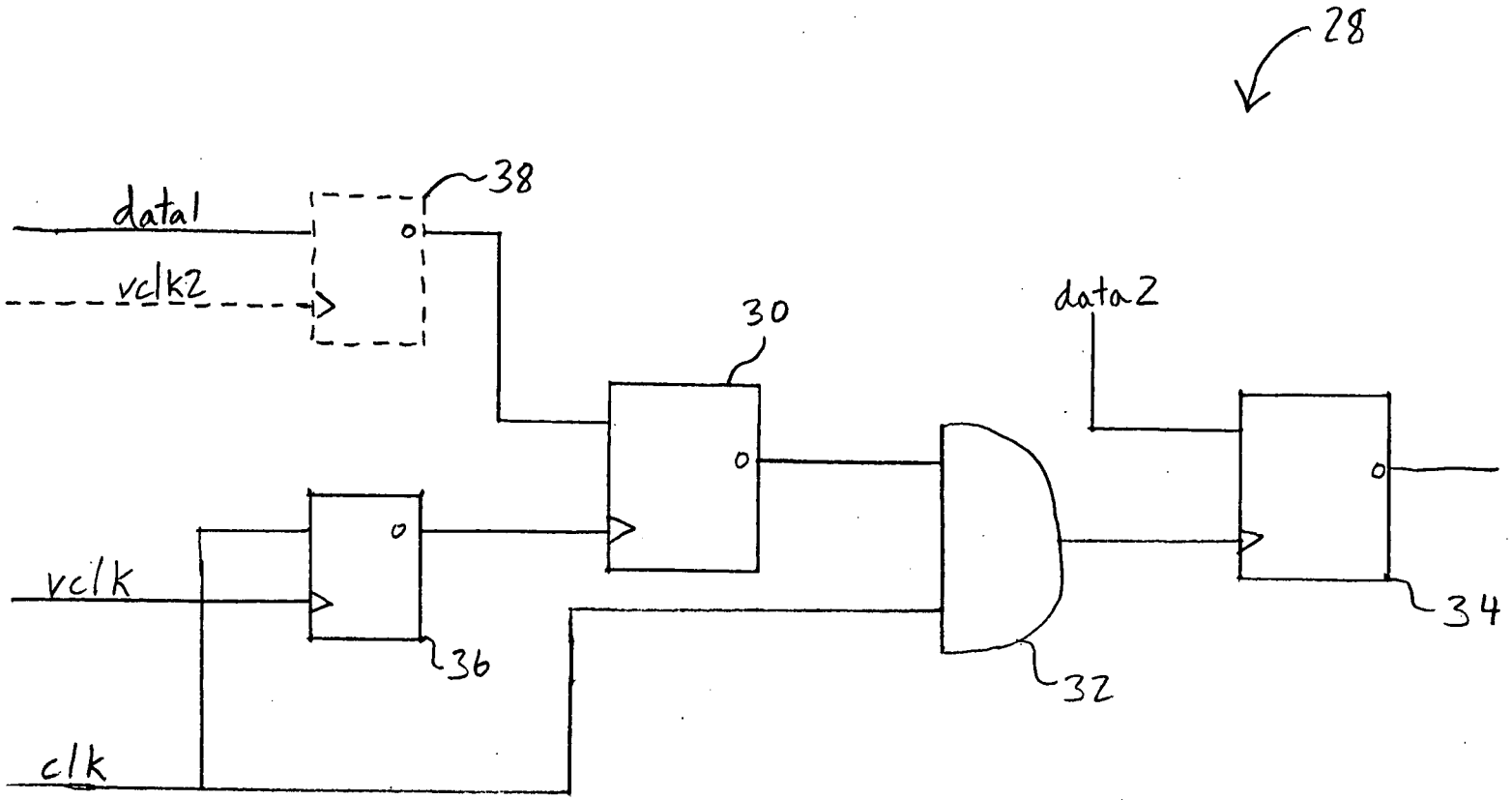


Fig. 4

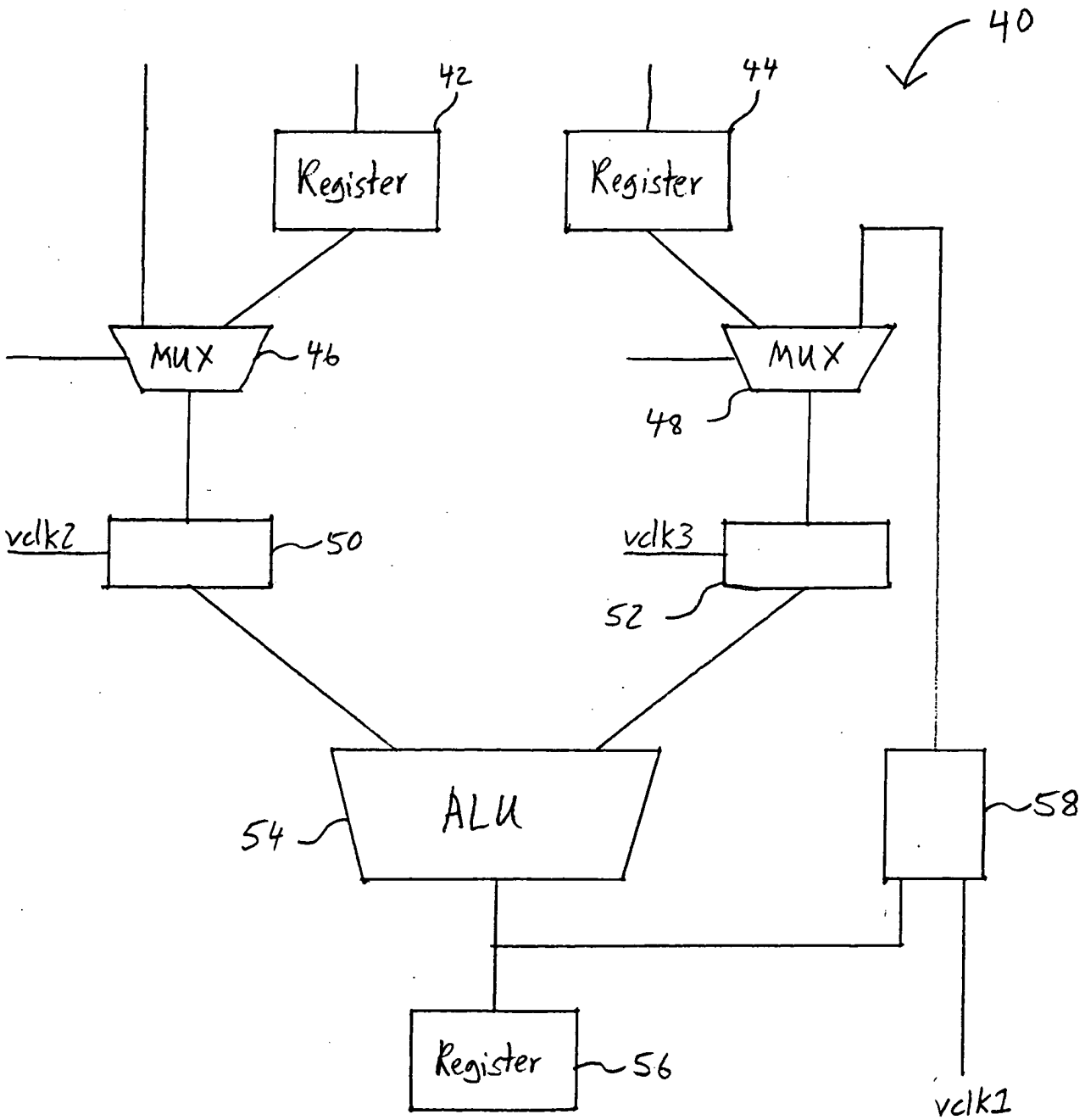
40
42
44
Register
Register
MUX
46
MUX
48
vclk2
50
vclk3
52
ALU
54
58
Register
56
vclk1

Fig. 5

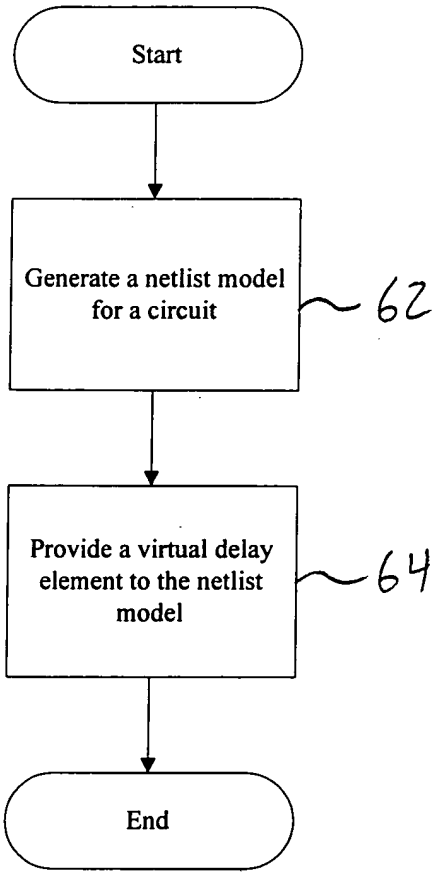
60
Start
Generate a netlist model for a circuit
62
Provide a virtual delay element to the netlist model
64
End

Figure 6